REMARKS

Claims 1 - 9, 19 - 38 and 42 - 44 remain active in this application. Non-elected claims 10 - 18 and claims 39 - 41 have been canceled. The claims have been reviewed and editorial revisions made where seen to be appropriate and further amended to be directed to embodiments characterized by connected discrete component which may be included in a single device package, consonant with the election of species previously made. No new matter has been introduced into the application. The indication of allowability of claims 23, 24 and 26 - 31 is noted with appreciation.

The Examiner has indicated that the previously submitted drawing revisions have been approved but raises additional objections to the drawings. In response, a further Request for Approval of Drawing Revisions is being concurrently filed herewith which addresses all the additional matters raised by the Examiner. Accordingly, the objections to the drawings are respectfully traversed as being moot in view of the proposed drawing revisions.

The Examiner has objected to claims 1, 19, 22, 25, 32, 33, 39, 40 and 41 for various informalities. This objection is similarly traversed as being moot in view of the amendments made above which are believed to address all of the Examiner's criticisms. Accordingly, reconsideration and withdrawal of the objection is respectfully requested.

Claims 40 - 44 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is also traversed as being moot in view of the amendments made above. Specifically, claims 39 - 41 have been cancelled as being unnecessary and largely redundant and the preamble of claims 42 - 44 have been amended to correspond to claim 33. Therefore,

reconsideration and withdrawal of this rejection is respectfully requested.

Claims 32 and 33 - 38 and 40 - 44 have been rejected under 35 U.S.C. §112, first paragraph; the Examiner criticizing the recital of the operation of the device in response to voltages applied and the connection of a capacitor. This rejection is respectfully traversed. The entire disclosure is directed to a three-terminal device including a thyristor in which a voltage of one polarity will turn the transistor on and a voltage of zero or and opposite polarity will turn the thyristor off. The capacitor connection in parallel to one of the transistors is shown in several Figures and clearly described in the specification. Therefore, it appears that the Examiner is, in fact, criticizing the recitation of the application of a signal to both the first and second transistors/switches and the recitation of a diode in the connection of the capacitor. Claims 32 and 33 have been suitably clarified. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 1 - 6, 8, 33, 34, 37 and 42 have been rejected under 35 U.S.C. §102 as being anticipated by Schlangenotto and claims 35, 36 38, 43 and 44 have been rejected under 35 U.S.C. §103 as being unpatentable over Schlangenotto. These grounds of rejection are also respectfully traversed as being moot in view of the amendments made above.

While Schlangenotto is similar in some respects to the circuit shown in Figure 1B of the application, the species shown in other Figures are quite different. Moreover, in regard to the amendments made above, Schlangenotto is directed to a device which is entirely integrated on a substrate and does not teach or suggest anything concerning provision of a thyristor device which is easily controlled even in a high current

conduction state and formed of discrete components by which particularly high current operation can be achieved. Since all claims have been amended to recite a device formed of discrete components, it is respectfully submitted that the rejections are no longer tenable and reconsideration and withdrawal of these rejections is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

A petition for a one-month extension of time has been made above. If any further extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

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APPENDIX

Claims 1, 19, 22, 23, 25, 32, 33 and 39 - 44:

1. (Twice Amended) An emitter controlled thyristor device package having a cathode terminal and an anode terminal, comprising:

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

a first discrete metal oxide semiconductor transistor (MOS) connected in series with said thyristor between said cathode terminal and said thyristor emitter[, said first MOS transistor integrated in at least one of the semiconductor regions of said thyristor];

a second discrete MOS transistor [integrated in at least one of said semiconductor regions] connected between said cathode terminal and said thyristor gate, a gate terminal of said second MOS transistor connected to said cathode terminal; and

means for injecting electrons into said thyristor for triggering said thyristor into [said] a latching state;

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode terminal turning said emitter controlled thyristor device to an on state, and a zero to second voltage [turns] applied to said gate of said first MOS transistor turns said emitter controlled thyristor device to an off state.

19. (Twice Amended) [An] A gate turn-off (GTO) thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal plate;

a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said GTO thyristor device package;

a first discrete metal oxide semiconductor (MOS) transistor positioned on said second metal plate adjacent said thyristor, said first MOS transistor having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for said [ETO] GTO device package; and

a second discrete MOS transistor positioned on said second metal plate adjacent said thyristor, said second MOS transistor having a first terminal connected to a gate of said thyristor, said second MOS transistor further having a second terminal and a gate terminal connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns said [emitter controlled] thyristor device to an off state.

22. (Amended) A gate turn-off (GTO) thyristor device package as recited in claim 39, wherein said first and second discrete semiconductor switches are first and second MOS transistors, respectively, and said first MOS transistor and said second MOS transistor are complementary.

23. (Amended) A gate turn-off thyristor (GTO) device package comprising:

a gate turn-off (GTO) thyristor comprising a

thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a first plurality of discrete [MOS transistors] switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said MOS transistors connected to said thyristor emitter and a second terminal of said MOS transistors connected to a cathode terminal of said GTO device package; and

a second plurality of discrete switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said [MOS] switching devices connected to said thyristor gate and a second terminal of said switching devices connected to said cathode terminal of said GTO device package,

wherein a first voltage applied to a gate terminal of said [MOS transistors] first plurality of switching devices turns said GTO thyristor to an on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate of said [MOS transistors] first plurality of switching devices turns said GTO thyristor to an off state.

25. (Twice Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 further comprising a third metal plate forming [and] an anode terminal of said GTO thyristor device package.

32. (Amended) A gate turn-off thyristor (GTO) as recited in claim 23, further wherein said [MOS] first switching [device comprises] devices comprise a MOS transistor comprising:

a feedback path connecting said gate terminal of said MOS [transistors] transistor to said thyristor emitter;

a capacitor connected in parallel to said [second feedback path] MOS switching device connecting said [gate] second terminal of said MOS [transistors] transistor to said thyristor gate terminal [through a diode].

33. (Twice Amended) An emitter turn-off thyristor device package including

a thyristor [device] element having an anode terminal, [a cathode] an emitter terminal and a gate terminal,

a first discrete semiconductor switch connected in series with said [cathode] emitter terminal of said thyristor device by a first terminal of said first semiconductor switch,

[as] a second discrete semiconductor switch connected in series with said gate terminal of said thyristor device by a first terminal of said second discrete semiconductor switch; second terminals of said first and second discrete semiconductor switches being connected together, and

means for shorting said emitter of said thyristor element to a terminal of said first discrete semiconductor switch or for injecting electrons into said thyristor for triggering said thyristor into [said] a latching state;

wherein said first and second discrete semiconductor switches are arranged such that a signal of a first type applied to said first [and second] discrete electronic [switches turn] switch turns said emitter turn-off thyristor to an on-state and a signal of a second type applied to said first [and second] electronic [switches turn] switch turns said emitter turn-off thyristor to an off-state.

41. (Amended) A GTO device package as recited in claim 19, wherein one of said first and second discrete

[switches is] MOS transistors includes a zener diode.

42. (Amended) [A GTO] An emitter turn-off device package as recited in claim 33, wherein one of said first and second discrete semiconductor switches [is] includes MOS transistor.

43. (Amended) [A GTO] An emitter turn-off device package as recited in claim 33, wherein one of said first and second discrete semiconductor switches [is] includes a diode.

44. (Amended) [A GTO] An emitter turn-off device package as recited in claim 33, wherein one of said first and second discrete semiconductor switches [is] includes a zener diode.